Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 4. This sheet, which includes Figure 4 and Figure 5, replaces the original sheet including Figure 4 and Figure 5.

The attached sheet of drawings includes changes to Figures 6a and 6b. This sheet, which includes Figures 6a, 6b, 7a and 7b, replaces the original sheet including Figures 6a, 6b, 7a and 7b.

The attached sheet of drawings includes changes to Figure 13. This sheet replaces the original sheet including Figure 13.

Attachment: 3 Replacement Sheets

Remarks

Applicant thanks the Examiner for finding claims 11-13 allowable if rewritten in independent form.

Claim 2 has been cancelled from the application, and new claims 30 and 31 have been added to the application. Claims 1, 3-14 and 23-30 are pending.

Objection to drawings

The Examiner objected to the drawings for failing to show the field oxide region recited in claim 2. In response, Figure 4 has been amended to show field oxide regions 113 that are grown adjacent to the diffusion region 110 and optional diffusion region 112. The description relating to Figure 4 has been amended to briefly describe the presence of the field oxide regions 113 for the embodiment of Figure 4.

Applicant notes that the corresponding plan view of the anti-fuse transistor 100 shown in Figure 5 shows the optional diffusion region extending to the right of polysilicon gate 106, therefore the field oxide region 113 will be understood to surround the active area and the diffusion regions 110 and 112. In the embodiment shown in Figure 12, persons skilled in the art will understand that the optional diffusion area 112 is not formed, therefore the area between adjacent anti-fuse transistors along the bitline direction will have field oxide regions grown. More specifically, persons skilled in the art will understand that the field oxide will extend from a bottom edge of the active region of the upper anti-fuse transistor (under polysilicon WL1) to the top edge of the active region of the bottom anti-fuse transistor (under polysilicon WL2). Applicant submits that no new subject matter is being added to the application.

The Examiner objected to the drawings for failing to show the low voltage transistor recited in claim 3 and the high voltage transistor recited in claim 4. In response, Applicant submits that the low voltage transistors are shown in Figures 11a, 11b and 13 as column select transistors 706, 708, 710 and 712 and the high voltage transistor is shown as isolation transistors 704. The description at paragraph [0086] states:

*"It is noted that isolation transistors **704** are thick gate oxide transistors,".*

The description at paragraph [0070] states:

"In a typical CMOS process, the diffusion regions, LDD and channel implantation are different for thin gate oxide transistors and thick gate oxide transistors. According to an embodiment of the present invention, the diffusion regions, LDD and the thin gate oxide channel implantation of the anti-fuse transistors can be either type; the low voltage type corresponding to the thin gate oxide, or the high voltage type corresponding to the thick gate oxide (I/O oxide),".

Accordingly, the description associates a high voltage type of transistor as having a thick gate oxide and a low voltage type of transistor as having a thin gate oxide. Therefore, isolation transistor 704 being described as having a thick gate oxide transistor will be associated with that of a high voltage transistor.

The description at paragraph [0090] further states:

*"the thick gate oxide isolation transistors **704** are used to isolate the bit lines from the rest of the chip, including the sense amplifiers."*

In Figures 11a, 11b and 13, the "rest of the chip" includes column select transistors 706, 708, 710 and 712 and the sense amplifier 716. In the description, the Applicant specifically singles out the isolation transistors 704 as being high voltage transistors, therefore the column select transistors 706, 708, 710 and 712 are low voltage transistors having the thin gate oxide. Those skilled in the art will understand that since the memory array bitlines and wordlines are subjected to high voltages, isolation transistors 704 are used to protect the more sensitive low voltage transistors from the high voltages that can appear on the bitlines during programming. In the embodiment of Figure 15, the low voltage sense amplifier 904 is isolated from the high voltage (VPP) cross-coupled transistor latch 902. Persons skilled in the art will clearly understand that the sense amplifier will include low voltage transistors having thin gate oxides relative to the high voltage isolation transistors 906. Applicant has therefore amended the description to explicitly state what is inferable from the description as filed; that the column select transistors are low voltage transistors. Applicant submits that no new subject matter is being added.

The Examiner objected to the drawings for failing to show wordline decoding circuitry recited in claim 12. In response, Figure 13 has been amended to include a wordline decoder circuit, which includes wordline decoding circuitry made up of predetermined logic for selecting wordlines based on a received address. Applicant submits that no new matter has been added, since wordline decoder circuits are well known in the art in memory applications.

The Examiner objected to the drawings for failing to show a column select pass gate recited in claim 14. In response, Applicant notes that Figures 11a, 11b and 13 all clearly show column select pass gates 706, 708, 710 and 712 coupled to respective bitlines, via isolation transistors 704. The Examiner states that the column select signals are not coupled to the bitlines. In fact the column select signals, such as Y0 for example, are intended to be coupled to the gates of the column select signals for turning them on and off.

The Examiner objected to the drawings for failing to show a fusible edge greater than a width of the active channel area recited in claim 26. Applicant believes the Examiner is referring to claim 25, as claim 26 does not recite this feature. In response, Applicant has amended claim 25 to recite that the fusible edge has a length that is greater than the access edge. In the embodiments of Figures 7a and 7b, a fusible edge is identified with reference numeral 312 while the access edge is identified with reference numeral 310. The description teaches that the access edge, which can be described as having a length dimension, is smaller than the fusible edge.

The Examiner objected to the drawings for failing to show an isolation edge recited in claim 29. In response, claim 29 has been amended to delete the expression "isolation edge", and to clarify the claimed anti-fuse transistor by reciting that the field oxide is adjacent to the fusible area. Amended claim 29 is directed to an embodiment of the anti-fuse transistor shown in Figure 12 of the present application. In Figure 12, the anti-fuse transistor has a diffusion region connected to a bitline, a polysilicon gate (WL1 for example), and an active area 118 that ends underneath the polysilicon gate. This differs from the anti-fuse embodiment shown in Figure 5 where the active area 118 extends beyond the right side of polysilicon gate 106. The description at paragraph [0087] states:

> *"Figure 12 illustrates a layout configuration of four anti-fuse transistors* ***702*** *shown in Figure 11a. Each anti-fuse transistor of Figure 12 have a layout*

*similar to anti-fuse transistor **100** shown in Figure 5, except that there is no floating source diffusion region to reduce the overall area of each cell."*

Accordingly, there is field oxide adjacent to the bottom edge of active area 118 covered by WL1, which should be well understood by any person skilled in the art. Applicant submits that claim 29 does not recite new subject matter, and the features recited therein are shown in the drawings.

The Examiner requested that the drawings be amended to label "edge segments" mentioned in the description. In response, Figures 6a and 6b have been amended to include reference number 209 to label the edge segments. The description relating to Figures 6a and 6b has been correspondingly amended to make reference to edge segments 209.

Claim rejections under 35 U.S.C. 112

The Examiner rejected claim 25 for reciting subject matter that is not supported by the description. In response, Applicant has amended claim 25 to recite that the fusible edge length is greater than a length of the access edge. As previously discussed, this claimed subject matter is supported by the embodiments of Figures 7a and 7b. Applicant submits that claim 25 is supported by the description of the application as filed, and withdrawal of the Examiner's rejection under 35 U.S.C. 112 is respectfully requested.

In response to the Examiner's rejection of claim 29 for reciting the feature "an isolation edge", claim 29 has been amended to delete the expression "isolation edge", such that the position of the field oxide is defined to be adjacent to the fusible area. Applicant submits that claim 29 is supported by the description of the application in the response to the Examiner's previous rejection to claim 29.

The Examiner rejected claim 3 as being indefinite as the expression *"the thin gate oxide portion is identical to at least one low voltage transistor gate oxide formed on the semiconductor material,"* may not be well understood. In response, claim 3 has been amended to clarify that the thin gate oxide portion corresponds to a gate oxide of a low voltage transistor formed elsewhere on the same semiconductor material as the anti-fuse transistor of claim 1. Applicant requests withdrawal of the Examiner's rejection under 35 U.S.C. 112.

The Examiner rejected claim 4 as being indefinite as the expression *"the thick gate oxide portion is identical to at least one high voltage transistor gate oxide formed on the semiconductor material,"* may not be well understood. In response, claim 4 has been amended to clarify that the thick gate oxide portion corresponds to a gate oxide of a high voltage transistor formed elsewhere on the same semiconductor material as the anti-fuse transistor of claim 1, and the low voltage transistor of claim 3. Applicant requests withdrawal of the Examiner's rejection under 35 U.S.C. 112.

The Examiner rejected claim 8 as being indefinite since the recitation of the LDD implant may not be well understood. In response, claim 8 has been amended to clarify that the LDD implant corresponds to the LDD implant of any one of the low voltage transistor of claim 3, the high voltage transistor of claim 4, and a combination LDD implant of the high and low voltage transistors. Applicant requests withdrawal of the Examiner's rejection under 35 U.S.C. 112.

The Examiner rejected claim 14 as being indefinite since the recitation of the thick gate oxide of the column select pass gate may not be well understood. In response, claim 14 has been amended to recite that the pass gate has a gate oxide that corresponds to the thick gate oxide portion of the anti-fuse transistor recited in claim 10. Applicant requests withdrawal of the Examiner's rejection under 35 U.S.C. 112.

Claim rejections under 35 U.S.C. 102

Rejection to claim 1

The Examiner rejected claim 1 as being anticipated by US Patent Publication No. 2004/0156234 (Peng). In particular, the Examiner believes that the Peng diffusion region between two adjacent memory cells shown in Figure 16 is analogous to the recited "isolation region" recited in claim 1. Claim 2 of the present application recites a further limitation where the isolation region includes a floating diffusion region and a field oxide region. While the Applicant disagrees with the Examiner that the Peng diffusion region is a floating diffusion region, the Examiner is silent on the limitation of the isolation region being a field oxide region.

Applicant submits that Peng does not teach or disclose an anti-fuse memory cell having a field oxide region proximate to a second end of the channel region. In claim 1, the second end of

the channel region is proximate to the thin gate oxide portion of the variable thickness gate oxide. In Figures 16 and 22-25 of Peng, the diffusion region is proximate to the thin gate oxide portion of two adjacent memory cells, which corresponds to the recited second end of the channel region of claim 1. It is clear from Figures 16 and 22-25 of Peng that there is no field oxide proximate to the thin gate oxide portion, since diffusion regions are used instead.

In the rejection to claim 29, the Examiner states that the recited field oxide is analogous to the LDD spacers formed beside the polysilicon gate shown in Peng. Respectfully, while LDD spacers are formed from oxide, they are not analogous in structure and function to field oxide. LDD spacers are well known drain engineering structures formed on the sides of the polysilicon gate and on the semiconductor surface to allow implantation of diffusion regions physically spaced from the edges of the polysilicon gates. Field oxide on the other hand is formed in the semiconductor surface to isolate the active area from other active areas. The Semiconductor Glossary at http://semiconductorglossary.com defines a spacer (as in an LDD spacer) as *"oxide deposited by CVD to isolate gate contact and source and drain contacts in MOSFETs; also passivates sidewalls of the gate stack."*. This glossary defines field oxide as *"relatively thick oxide (typically 100 - 500 nm) formed to passivate and protect semiconductor surface outside of active device area; part of any semiconductor device, but does not participate in device operation."*. The field oxide is a unique and well known structure that is different than the well known LDD spacer, and are therefore not analogous to each other.

Therefore, in view of the novelty of this recited feature in claim 2, Applicant has amended claim 1 to specifically recite that there is a field oxide region proximate to a second end of the channel region, which is not disclosed, taught or inferred by Peng. Applicant therefore submits that amended claim 1 is not anticipated by Peng, and claims 3 to 9 which depend either directly or indirectly from amended claim 1 are therefore not anticipated by Peng. Applicant respectfully requests withdrawal of the rejection to claims 1-9 under 35 U.S.C. 102.

Rejection to claim 3

Claim 3 recites that the thin oxide portion of the anti-fuse transistor corresponds to the gate oxide of a low voltage transistor formed on the same semiconductor material. The Examiner rejected claim 3 as he believes that the recited limitations are described in paragraph [0091] of Peng. Applicant respectfully disagrees, and submits that the thin oxide portion of the Peng anti-fuse transistor does not correspond to the gate oxide of a low voltage transistor. In fact,

Peng teaches that the thick oxide portion of the anti-fuse transistor corresponds to the gate oxide of the low voltage transistor.

Peng states at paragraph [0091] that *"the transistors used in the memory cells are normal low voltage logic transistors having, for example, an ultra-thin gate oxide thickness on the order of…20A for a 0.13 μm process."*. Figure 21 shows a stage during the fabrication of the Peng anti-fuse transistor which is described at paragraph [0085], where *"a normal gate oxidation is performed to grow 20A (for 0.13μm generic process) on the non-nitrogen implanted area. At the same time, a 10 to 15A thinner gate oxide will be grown in the nitrogen implanted silicon region."*. Peng previously states in paragraph [0083] that nitrogen is used to reduce silicon oxidation, thereby resulting in the thinner 10 to 15A gate oxide. In Figure 21, Peng labels the thicker portion of the gate oxide as the "Normal gate oxide thickness", and the thinner portion as the "Thinner gate oxide thickness". In Figure 22 which shows the substantially completed memory cells, Peng once again labels the thicker portion of the gate oxide as the "Normal gate oxide thickness", and the thinner portion as the "Thinner gate oxide thickness".

Therefore, Peng teaches that the normal gate oxide of a low voltage transistor is 20A and the thick gate oxide portion of the anti-fuse transistor is a normal gate oxide thickness of 20A. Therefore the Peng thin oxide portion does not correspond to the gate oxide of the low voltage transistor, which Peng teaches to be between 10 to 15A. Applicant submits that claim 3 is not disclosed, taught or inferred by Peng, and withdrawal of the Examiner's rejection under 35 U.S.C. 102 is respectfully requested.

Rejection to claim 4

Claim 4 recites that the thick oxide portion of the anti-fuse transistor corresponds to the gate oxide of a high voltage transistor formed on the same semiconductor material. The Examiner rejected claim 4 as he believes that the recited limitations are described in paragraphs [0008] and [0010] of Peng. Applicant respectfully disagrees. Firstly, the argument presented above clearly shows that the Peng anti-fuse transistor has a thick gate oxide portion that corresponds to the gate oxide of a low voltage transistor. Secondly, paragraphs [0008] and [0010] of Peng merely discuss the state of the prior art, and only make mention of high voltage circuits. Nowhere do these paragraphs state or infer that an anti-fuse transistor has a thick gate oxide portion that corresponds to a thick gate oxide of a high voltage transistor. Applicant therefore

submits that claim 4 is not disclosed, taught or inferred by Peng, and withdrawal of the Examiner's rejection under 35 U.S.C. 102 is respectfully requested.

Rejection to claim 6

The Examiner rejected claim 6 which adds further features to the anti-fuse transistor recited in claim 1. These being the limitation that there is a common edge shared by the floating diffusion region, second end of the channel region and a gate edge of the polysilicon gate, which is defined by at least two line segments being at an angle to each other. Claim 6 is directed to the embodiment of the invention shown in Figure 6A of the present application. Applicant submits that this limitation is not disclosed or taught in Peng. Peng shows in Figure 19 that the polysilicon gates which extend vertically have a single segment that spans a width dimension of the transistor active area. Peng does not show any structure remotely similar to that recited in claim 6. Therefore, withdrawal of the Examiner's rejection to claim 6 and dependent claim 7 under 35 U.S.C. 102 is requested.

Rejection to claim 24

The Examiner rejected claim 24 which adds further features to the anti-fuse transistor recited in claim 23. This limitation is similar to the limitation recited in claim 6, which is not disclosed or taught in Peng. Therefore, withdrawal of the Examiner's rejection to claim 24 under 35 U.S.C. 102 is requested.

Rejection to claim 29

In the Examiner's anticipation rejection to claim 29, an LDD spacer is cited by the Examiner as being analogous to the recited field oxide. Claim 29 has been amended to recite that the field oxide is adjacent the fusible area, and Applicant submits that the LDD spacer is a different structure that is both structurally and functionally different than a field oxide. As previously mentioned, the LDD spacer is used for drain engineering purposes and is formed on the semiconductor surface. The field oxide on the other hand, is formed within the semiconductor surface to isolate active areas, which include channel, drain and source diffusion regions, from other such active areas. Therefore, since the feature whereby field oxide adjacent to the fusible area is not disclosed or taught by Peng, Applicant requests withdrawal of the rejection to claim 29 under 35 U.S.C. 102.

New claim

Applicant has added new claim 30 to the application. New claim 30 substantially corresponds to claim 1, and recites the limitations recited in dependent claims 3 and 4. Applicant submits that new claim 30 is novel and not anticipated by Peng since Peng does not teach, disclose or infer that the thick gate oxide portion corresponds to the gate oxide of a high voltage transistor while the thin gate oxide portion corresponds to the gate oxide of a low voltage transistor. As previously argued, the Peng anti-fuse transistor has a thick gate oxide portion that corresponds to a low voltage transistor. New claim 31 substantially corresponds to cancelled claim 2, and recites further limitations of the anti-fuse transistor of claim 30.

The Examiner is invited to call Shin Hung at (613)787-3571 should he wish to discuss the presented amendments, or to discuss the presented arguments.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

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Att.

3 Replacement Sheets (Figures)